REMARKS

Claims 1-12 are presented for examination. Claims 1-8 have been rejected under 35 U.S.C. 102(b) as being anticipated by Inagaki. Dependent claims 9-12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Inagaki in view of Taguchi.

These rejections are respectfully traversed for the following reasons.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989).

Independent claim 1 recites a semiconductor memory device that comprises:

-a memory array including a plurality of memory cells arranged in a matrix;

-a refresh timer circuit providing a refresh request signal at a time interval required to refresh data held by said plurality of memory cells;

-a command generation circuit generating an internal command signal in response to an access command; and

-a row selection control circuit carrying out an operation associated with row selection of said memory array.

The row selection control circuit includes:

- a timing control circuit rendered active in response to said internal command signal to output a timing signal of a row selection operation of said memory cell,

- a refresh control circuit receiving and holding said refresh request signal to output an internal refresh command signal when said timing control circuit attains an inactive state, and

- a refresh timing control circuit rendered active in response to said internal refresh command signal to output said timing signal instead of said timing control circuit.

The Examiner takes the position that:

- timing signal generator 25 (FIG. 1 of Inagaki) corresponds to the claimed timing control circuit, and address latch signal AL corresponds to the claimed timing signal.

- refresh timing circuit 28 corresponds to the claimed refresh control circuit, and

- the timing signal generator 25, timer 30 and timer control 32 correspond to the claimed refresh timing control circuit.

As demonstrated below, Inagaki neither expressly nor under the principles of inherency discloses the following claimed elements:

-the refresh control circuit receiving and holding said refresh request signal to output an internal refresh command signal when said timing control circuit attains an inactive state, and

-the refresh timing control circuit rendered active in response to said internal refresh command signal to output said timing signal instead of said timing control circuit.

Considering the reference, Inagaki discloses that the refresh timing circuit 28 (considered by the Examiner to correspond to the claimed refresh control circuit) generates an internal refresh control signal RF supplied to the timing signal generator 25 to produce a row-decoder activating signal XE and a sense enabling signal SE. However, the refresh

timing circuit 28 does not hold the refresh signal RFSH/ to output the signal RF when the timing signal generator 25 (considered by the Examiner to correspond to the claimed timing control circuit) attains an inactive state, as the Examiner asserts.

Accordingly, Inagaki does not disclose the claimed refresh control circuit receiving and holding the refresh request signal to output an internal refresh command signal when the timing control circuit attains an inactive state.

Further, the reference contains no teaching of any timing circuit that would be activated by the signal RF to output the signal AL (or any other timing signal) instead of the timing signal generator 25.

It is noted that the Examiner takes the position that the timing signal generator 25 acts at the same time as the timing control circuit, and as the refresh timing control circuit, which produces the timing signal instead of the timing control circuit. This position is improper because the same signal generator cannot operate as a regular timing control circuit and as a refresh timing control circuit producing timing signal instead of the regular timing control circuit.

Hence, Inagaki does not disclose the claimed refresh timing control circuit rendered active in response to the internal refresh command signal to output the timing signal instead of the timing control circuit.

In the event the Examiner relied upon inherency without expressly indicating such reliance, the Examiner should be aware that inherency requires certainty, not speculation. ***In re Rijckaert***, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); ***In re King***, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); ***W. L. Gore & Associates, Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); ***In re Oelrich***, 666 F.2d 578, 212 USPQ 323 (CCPA

1981); ***In re Wilding***, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

However, the Examiner provided no factual basis upon which to conclude that Inagaki contains the refresh control circuit and the refresh timing control circuit operating in the manner required by claim 1.

Moreover, one skilled in the art would understand that Inagaki discloses an integrated circuit 10 (FIG. 1) receiving an external refresh signal /RFSH. The integrated circuit 10 rejects external command when it receives instructions to switch its operation mode to the refresh mode.

By contrast, the semiconductor memory device of the present invention does not receive the refresh entry mode signal from outside. Instead, it generates an internal refresh request signal, and arbitrates between the refresh request signal and external commands to perform internal refresh.

Therefore, one skilled in the art would understand that Inagaki does not need the refresh control circuit and the refresh timing control circuit operating in the manner required by claim 1.

Accordingly, Inagaki neither expressly nor under the principles of inherency discloses the arrangement recited in claim 1. Therefore, the reference does not describe the claimed invention within the meaning of 35 U.S.C. § 102.

Dependent claims 2-12 are defined over the prior art at least for the reasons presented above in connection with claim 1. Applicants, therefore, respectfully submit that the rejection of claims 1-8 under 35 U.S.C. 102(b) as being anticipated by Inagaki, and claims 9-12 under 35 U.S.C. 103(a) as being unpatentable over Inagaki in view of Taguchi. are untenable and should be withdrawn.

In view of the foregoing, and in summary, claims 1-12 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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